Form PTO-1449 (modified)	ATTY. DKT. NO. 5681-67300	SERIAL NO. 10/696,891
List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	APPLICANT: Robert E. Cypher FILING DATE: October 30, 2003	GROUP: 2131

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

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	A9	"Error Correction with Hamming Codes," http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/hamming.htm, 1994, 2 pgs.
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	A11	Barker et al., "Hamming Code, Theory," http://www.eng2.uconn.edu/cse/Courses/CSE208W/ Hamming/Theory.html, March 1998, 2 pgs.
	A12	"NUMA: Delivering the Next Level of Commodity SMP Performance," http://199.245.235.23/ newsletters/html/vpoint5.html, 1996, 4 pgs.
	A13	Barker et al. "General Definitions," http://www.eng2.uconn.edu/cse/Cour...8W/References/ Ref_Definitions.html, February 1998, 3 pgs.
	A14	Barker et al. "Hamming Code, Lab Procedure," http://www.eng2.uconn.edu/cse/Courses/CSE208W/ Hamming/Procedure.html, June 1998, 3 pgs.
	A15	Burskirk, "32-Bit-Wide Memory Tolerates Failures," NT Tech Notes, October 1990, p. 818.
	A16	C. L. Chen, "Symbol Error Correcting Codes for Memory Applications," IBM Corporation, IEEE, 1996, pages 200-207.
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	A18	Hamada, et al., "A Class of Error Control Codes for Byte Organized Memory Systems -SbEC-(Sb+S)ED Codes-," IEEE Transactions of Computers, Vol. 46, No. 1, January 1997, 5 pages.
	A19	Costello, Jr., et al., "Applications of Error-Control Coding," IEEE Transactions on Information Theory, Vol. 44, NO. 6, October 1998, pages 2531-2560.
	A20	Ziegler, et al., "Cosmic Ray Soft Error Rates of 16-Mb DRAM Memory Chips," IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998, pages 246-252.
	A21	Peterson, et al., "Error-Correcting Codes," Second Edition, The MIT Press, 1972, pages 357-373.
	A22	Shu Lin, "Error Control Coding, Fundamental and Applications," Prentice-Hall, 1983, pp. 503-525 and 532.

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	A9	"Error Correction with Hamming Codes," http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/hamming.htm, 1994, 2 pgs.
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	A12	"NUMA: Delivering the Next Level of Commodity SMP Performance," http://199.245.235.23/ newsletters/html/vpoint5.html, 1996, 4 pgs.
	A13	Barker et al. "General Definitions," http://www.eng2.uconn.edu/cse/Cour...8W/References/ Ref_Definitions.html, February 1998, 3 pgs.
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	A15	Burskirk, "32-Bit-Wide Memory Tolerates Failures," NT Tech Notes, October 1990, p. 818.
	A16	C. L. Chen, "Symbol Error Correcting Codes for Memory Applications," IBM Corporation, IEEE, 1996, pages 200-207.
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	A19	Costello, Jr., et al., "Applications of Error-Control Coding," IEEE Transactions on Information Theory, Vol. 44, NO. 6, October 1998, pages 2531-2560.
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	A21	Peterson, et al., "Error-Correcting Codes," Second Edition, The MIT Press, 1972, pages 357-373.
	A22	Shu Lin, "Error Control Coding, Fundamental and Applications," Prentice-Hall, 1983, pp. 503-525 and 532.

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Information Disclosure Statement--PTO 1449 (modified)

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U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
GL	B1	5,867,642	2/2/99	Vivio, et al.			
	B2	5,757,823	5/26/98	Chen, et al.			

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	B3	IBM Technical Disclosure Bulletin, "Memory Chip Failure-Detection Mechansim", March 1991, Vol. 33, No. 10A, XP000110029, pp. 240 - 242.
GL	B4	Saxena, et al., "Error Detection and Handling in a Superscalar, Speculative Out-of-Order Execution Processor System," IEEE, 1995, pp. 464-471.
	B5	Rolf Johansson, "Two Error-Detecting and Correcting Circuits for Space Applications," IEEE 1996, pp. 436-439.
	B6	IBM Technical Disclosure Bulletin, "Concurrent On-Lin Array Chip Sparing From Scrub-Assisted Fault Data," December 1991, Vol. 34, No. 7A, pp. 16-19.

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
Stylesheet Version v18.0

Title of Invention	ECC for Component Failures Using Galois Fields

Application Number: 10/696891

Confirmation Number: 9249

First Named Applicant: Robert Cypher

Attorney Docket Number: 5681-67300

Art Unit: 2131

Search string: (5812564).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
GL	1	5812564	1998-09-22	Bonke et al			

Signature

Examiner Name	Date
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ATTY. DKT. NO. 5681-67300

APPLICANT: Robert E. Cypher

FILING DATE: October 30, 2003

SERIAL NO. 10/696,891

GROUP: 2131

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	E1	2001/0001158	5/10/01	Tetrick			
	E2	6246616	6/12/01	Nagai, et al			
	E3	6233717	5/15/01	Choi			
	E4	6223301	4/24/01	Santeler, et al			
GL	E5	6209113	3/27/01	Roohparvar			
	E6	6181614	1/30/01	Aipperspach, et al			
	E7	6167495	12/26/00	Keeth, et al			
	E8	6158025	12/5/00	Brisse, et al			
	E9	6141789	10/31/00	Cypher			
	E10	6115828	9/5/00	Tsutsumi, et al			
	E11	6101614	8/8/00	Gonzales, et al			
	E12	6076182	6/13/00	Jeddeloh			
	E13	6065102	5/16/00	Peters, et al			
	E14	6044483	3/28/00	Chen, et al			
	E15	6070255	5/30/00	Dell, et al			
	E16	6052818	4/18/00	Dell, et al			
	E17	6038680	3/14/00	Olarig			
	E18	6018817	1/28/00	Chen, et al			
	E19	6009548	12/28/99	Chen, et al			
	E20	5987628	11/16/99	Von Bokern, et al			
	E21	5978952	11/2/99	Hayek, et al			
	E22	5953265	9/14/99	Walton, et al			
	E23	5928367	7/27/99	Nelson, et al			
	E24	5923682	7/13/99	Seyyedy			
	E25	5909541	6/1/99	Sampson, et al			
	E26	5872790	2/16/99	Dixon			
	E27	5822257	10/13/98	Ogawa			

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	E28	5758056	5/26/98	Barr			
	E29	5682394	10/28/97	Blake, et al			
	E30	5640353	6/17/97	Ju			
	E31	5502675	3/26/96	Kohno, et al			
	E32	5490155	2/6/96	Abdoo, et al			
	E33	5291496	3/1/94	Andaleon, et al			
	E34	5276834	1/4/94	Mauritz, et al			
GL	E35	5255226	10/19/93	Ohno, et al			
	E36	5233614	8/3/93	Singh			
	E37	5228046	7/13/93	Blake, et al			
	E38	5164944	11/17/92	Benton, et al			
	E39	5077737	12/31/91	Leger, et al			
	E40	5058115	10/15/91	Blake, et al			
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	E49	2003/0133611	12-2003	Humlicek et al.			
	E50	5,867,642	2/2/99	Vivio, et al.			
	E51	5,757,823	5/26/98	Chen, et al.			

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GL	E52	Polianskikh, B. et al., "design and Implementation of Error Detection and Correction Circuitry for Multilevel Memory Protection," Multiple-Valued Logic 2000. ISMVL 2002. Proceedings 32nd IEEE International Symposium on 5-18 May 2002, Pages 89-95
	E53	K. A. S. Immink, "A Practical Method for Approaching the Channel Capacity of Constrained Channels," September 1997, IEEE Transactions on Information Theory, Vol. 43, No. 5, Pages 1389-1399

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U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
GL		6,976,194	12/13/05	Cypher			
GL JAN 27 2006		6,996,766	2/7/06	Cypher			

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GL		6,973,613	12/6/06	Robert E. Cypher			

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		5,303,302	4/94	Michael Burrows			
		5,177,747	1/93	Capps, et al.			
		5,537,421	7/96	Dujari, et al.			
		5,606,662	2/97	Michael T. Wisor			
GL		6,779,150	8/04	Walton, et al.			
		6,766,493	7/20/04	Hoffman, et al.			
		6,738,947	5/18/04	Maeda			
		6,704,838	3/9/04	Anderson			
		6,374,383	4/16/02	Weng			
		4,433,388	2/21/84	Oosterbaan			
		5,020,060	5/28/91	Murai , et al.			
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	F2	Craig Partridge, et al., "Performance of Checksums and CRCs over Real Data," 1995 ACM, pp. 68-76.	
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	F11	Satran, Sheinwald Informational, "iSCSI CRC Considerations," May 7, 2001, 18 pages.	
	F12	"A Short Spiel on 1-Bit Error Correction Codes," printed 8/11/01, 2 pages.	
	F13	Rick Kelly, "Error Management Using DesignWare CRC and ECC," 2001 Synopsys, Inc., 5 pages.	
	F14	ZDNet UK, "Parity RAM and ECC," PC Magazine Guide to Servers, 1999, 1 page.	
	F15	"Before you start - Chapter 6: Break and Verify," © Laurence Soucy 1997/2001, 1 page.	
	F16	"A Painless Guide to CRC Error Dection Algorithms," Version 3.00, 9/24/96, 19 pages.	
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